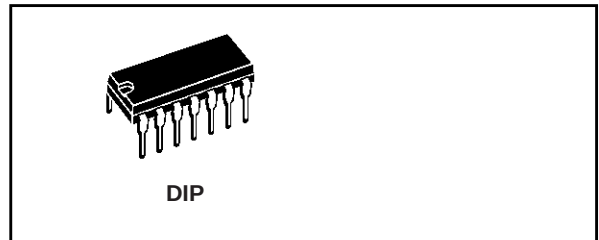




DUAL COMPLEMENTARY PAIR PLUS INVERTER

- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MEDIUM SPEED OPERATION
 $t_{PD} = 30\text{ns}$ (Typ.) AT 10V
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT
 $I_I = 100\text{nA}$ (MAX) AT $V_{DD} = 18\text{V}$ $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



ORDER CODES

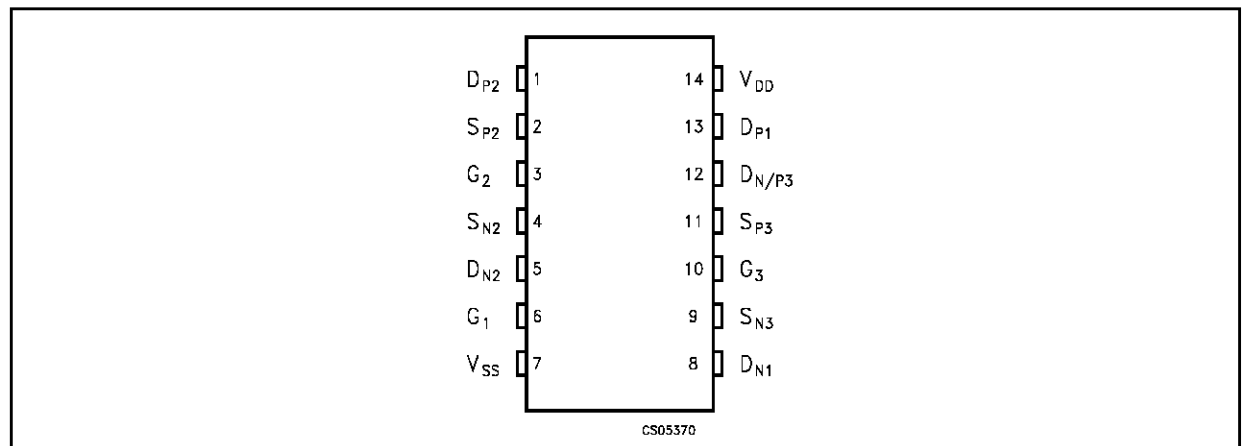
PACKAGE	TUBE	T & R
DIP	CC4007	

DESCRIPTION

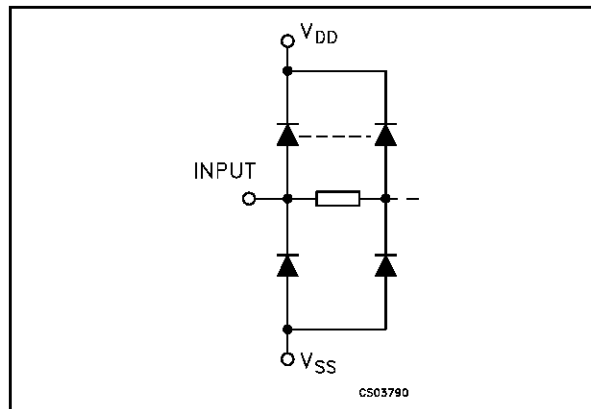
The CC4007 is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. The CC4007 type is comprised of three n-channel and three p-channel enhancement type MOS transistors. The transistor elements are accessible through the package terminals to

provide a convenient means for constructing the various typical circuits as shown in typical applications. More complex functions are possible using multiple packages. Number shown in parentheses indicate terminals that are connected together to form the various configuration listed.

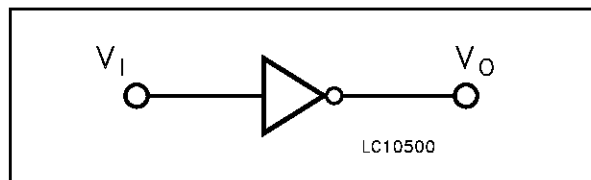
PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



LOGIC DIAGRAM



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
2, 11	S_{P2}, S_{P3}	Source Connections to 2nd and 3rd p-channel transistors
13, 1	D_{P1}, D_{P2}	Drain Connections from the 1st and 2nd p-channel transistors
8, 5	D_{N1}, D_{N2}	Drain Connections from the 1st and 2nd n-channel transistors
4, 9	S_{N2}, S_{N3}	Source Connections to the 2nd and 3rd n-channel
12	$D_{N/P3}$	Common connection to the 3rd p-channel and n-channel transistor drains
6, 3, 10	G_1 to G_3	Gate connections to n-channel and p-channel of the three transistor pairs
7	V_{SS}	Negative Supply Voltage
14	V_{DD}	Positive Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +20	V
V_I	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 18	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value								Unit
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I _L	Quiescent Current	0/5			5		0.01	0.25		7.5		7.5	μA	
		0/10			10		0.01	0.5		15		15		
		0/15			15		0.01	1		30		30		
		0/18			18		0.02	5		150		150		
V _{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V	
		0/10		<1	10	9.95			9.95		9.95			
		0/15		<1	15	14.95			14.95		14.95			
V _{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V	
		10/0		<1	10		0.05			0.05		0.05		
		15/0		<1	15		0.05			0.05		0.05		
V _{IH}	High Level Input Voltage		0.5/4.5	<1	5	4			4		4		V	
			1/9	<1	10	8			8		8			
			1.5/13.5	<1	15	12.5			12.5		12.5			
V _{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1		1		1	V	
			9/1	<1	10			2		2		2		
			13.5/1.5	<1	15			2.5		2.5		2.5		
I _{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
I _{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			
I _I	Input Leakage Current	0/18	Any Input		18		±10 ⁻⁵	±0.1		±1		±1	μA	
C _I	Input Capacitance		Any Input				5	7.5					pF	

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

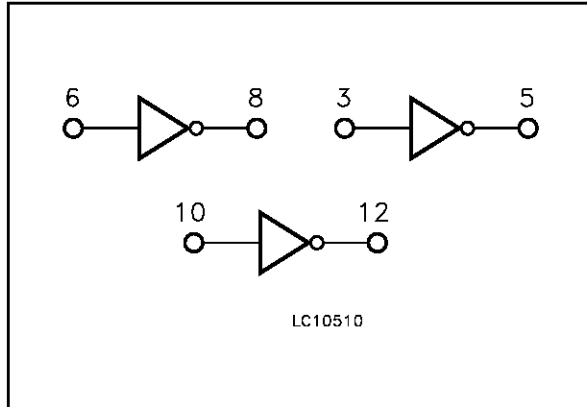
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200K Ω , t_r = t_f = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V _{DD} (V)		Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time	5			55	110	ns
		10			30	60	
		15			25	50	
t _{TLH} t _{THL}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

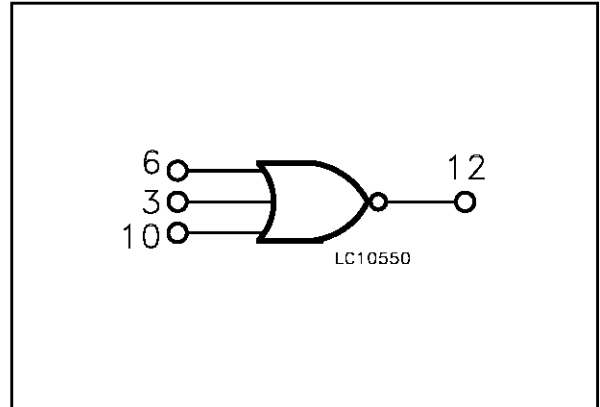
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.

TYPICAL APPLICATIONS

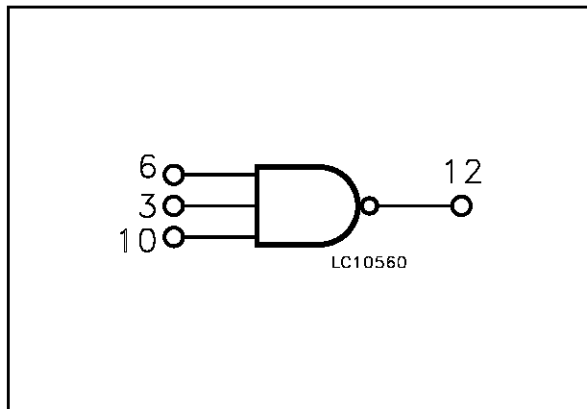
TRIPLE INVERTERS : (14, 2, 11); (8,13); (1, 5);
(4, 7, 9)



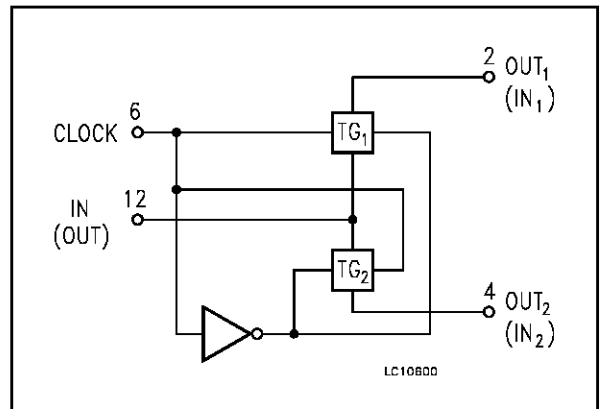
3-INPUT NOR GATE : (13, 2); (1, 11); (12, 5, 8);
(4, 7, 9)



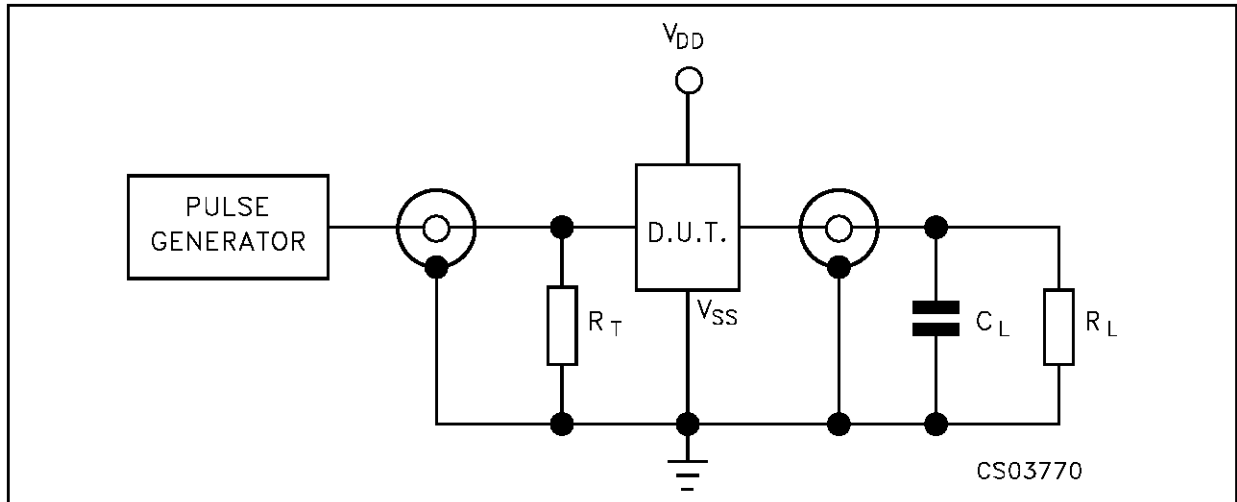
3-INPUT NAND GATE : (1, 12, 13); (2, 14, 11);
(4, 8); (5, 9)



DUAL BIDIRECTIONAL TRASMISSION GATING : (1, 5, 12); (2, 9); (11, 4); (8,13,10); (6, 3)



TEST CIRCUIT



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 200\text{k}\Omega$
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM : PROPAGATION DELAY TIMES ($f=1\text{MHz}$; 50% duty cycle)